A TRIP DOWN MEMORY LANE:

UPS, DOWNS AND WORKAROUNDS OF A TEST ENGINEER?

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TEST ACCESS, AUTOMATION, AND ADOPTION WORKSHOP 2021

KEYNOTE ADDRESS

ABOUT ME

- Started out as a aircraft mechanic with avionics and turbine engine specialties
- Joined robotics group of AT&T Western Electric designing robots and vision systems in 1982
- In 1989, I joined the Western Electric Test Engineering Department (Introduced to standards by Rod Tulloss)
- I've been working with test and standards ever since
- IEEE standards I have been a part of are 1149.1 (indirectly), 1532, 1581, 1687, 1149.7, P1687.1, P2654, P2929
- Spent 37 years developing advanced test technologies for AT&T, Lucent Technologies, Alcatel-Lucent, and Nokia (now as a Consultant)

WHAT MAKES A TECHNOLOGY SUCCESSFUL (OR NOT)? *IT'S UP TO YOU!*

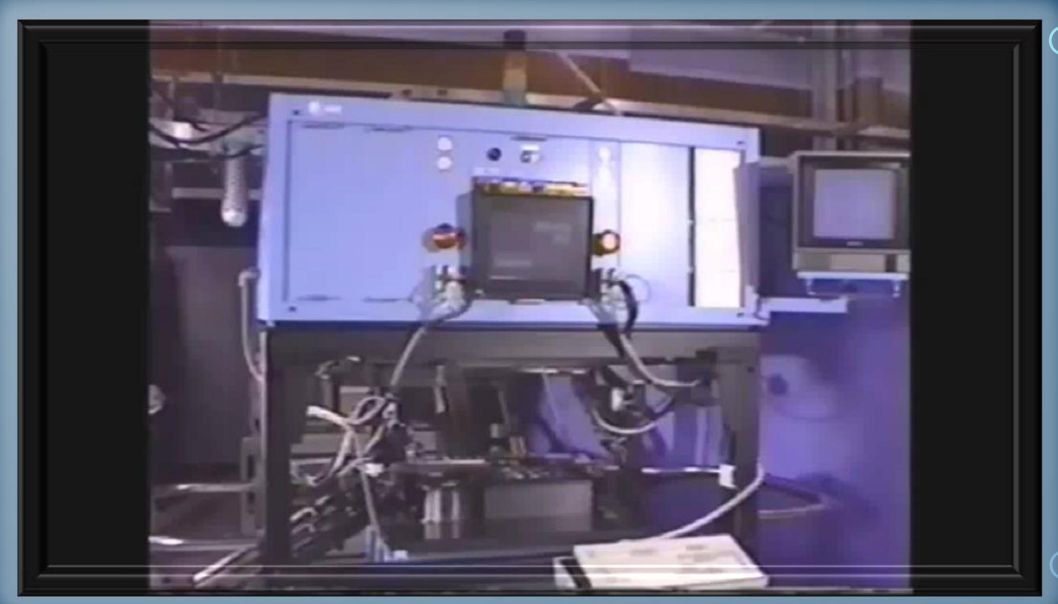
- Don't just use a technology, embrace it
- Look for ways to exploit it in your product
- Look at how it can be used for other applications
- Look for ways a technology may be extended or abstracted
- Look for ways to involve more people (user groups)
- Look for ways to standardize it
- Look for ways YOU can GROW to use it more intelligently
- Look at ways others are using it
- Look for ways to demonstrate HUGE savings (ROI)

WHAT MAKES A TECHNOLOGY SUCCESSFUL (OR NOT)? *IT'S UP TO YOU!*

- Whatever you do, make it complete and flexible
- If you can make a technology open and extensible, it will be used more
- Remember people will use the technology in more ways than you planned
- Accept feedback from others
- YOU don't have all the ideas
- Bounce ideas off others and be open to alternate perspectives
- Listen to other's about what they feel is missing in regards to what they want to do

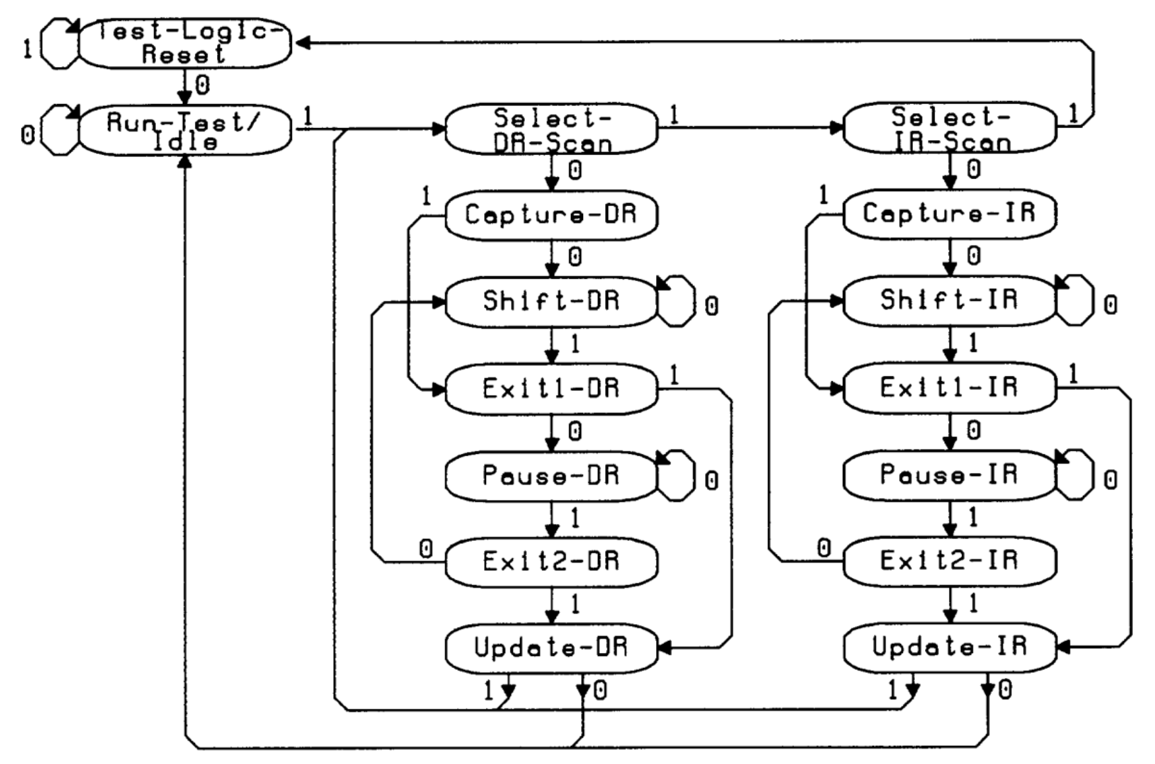
AT&T FLEXIBLE WORK STATION (FWS)

- First commercial robotic assembly operation using Bruce Sawyer's Linear Stepper Motor
- ✓ Used originally for pen plotters to draw very large topological maps
- ✓ Repurposed to move robot end effectors instead of pens
- ✓ Now used extensively for Flying Probe testers
- ➢ **Look outside of your industry at how other industries tackle similar problems**



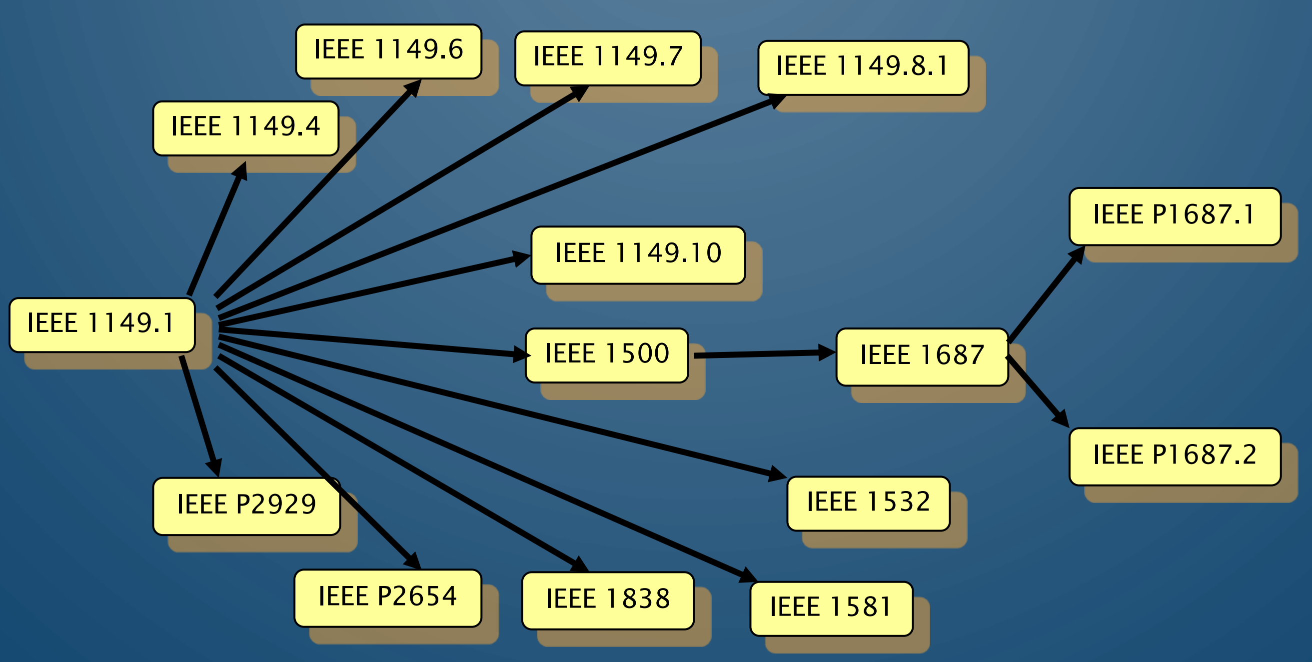
WHAT IS A TAP?

- *Pre-1988*
- *Post-1988*



JTAG Meeting, 17 September, 1988

OUT OF ONE IDEA: MANY HAVE BEEN CREATED

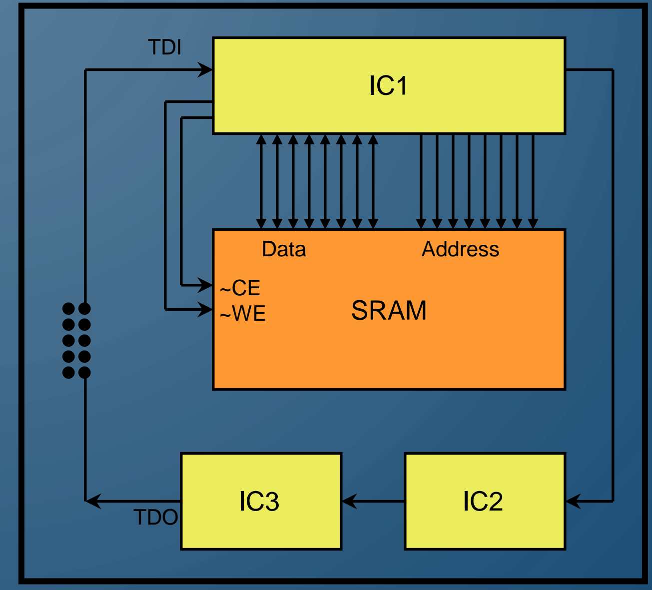


CLUSTER TEST FOR MEMORY AND LOGIC BLOCKS

- Use Boundary-Scan Register (BSR) of a device to test connections to one or more other devices
- Dedicated Memory Test tooling using read/write strategy
- Generalize process with domain specific languages (DSL) to test clusters of circuits with user specified strategy

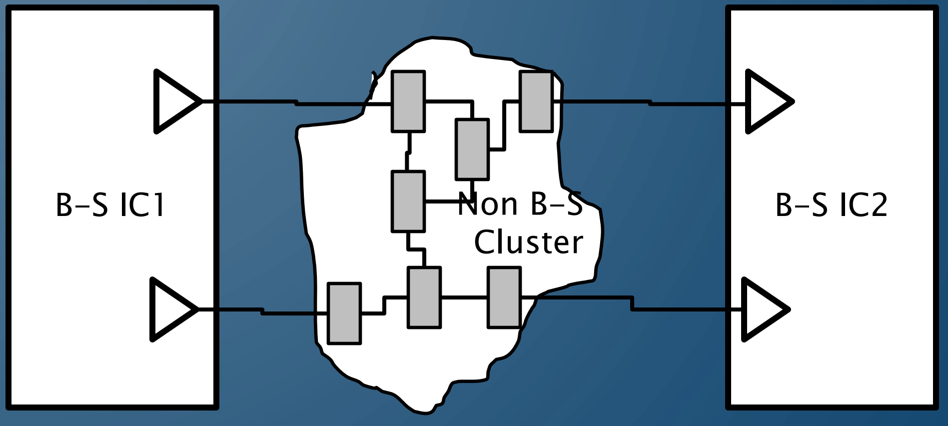
➢ **Generalize specific tooling to leverage concept for other applications**

Boundary-Scan Memory Cluster Test



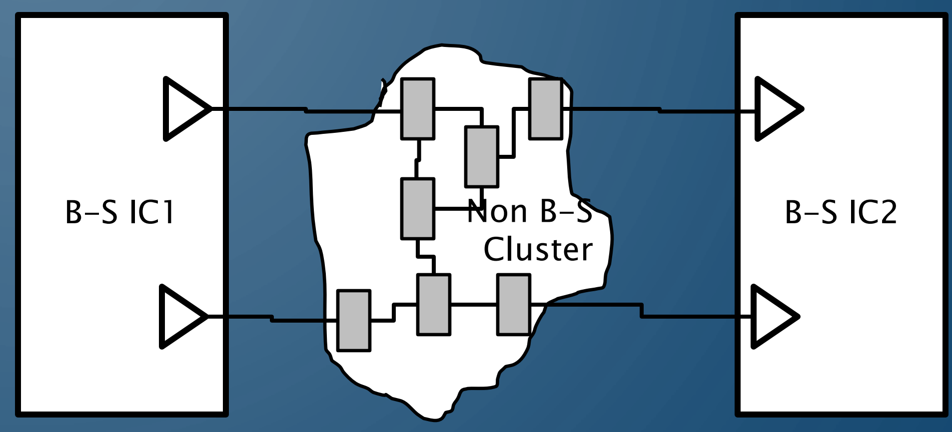
CLUSTER DIAGNOSTICS TOOL

- Surround cluster with Boundary-Scan Pins
- Diagnose faults inside cluster
- Uses back propagation from output to input for each level (leverage ASIC back propagation tool)
- Requires modeling of internal cluster logic



CLUSTER DIAGNOSTICS TOOL

- Worked well when models for cluster devices available
- Difficult to find models for most target clusters
- Clusters ended up being too complex to model by hand and not available from vendors



DSL-BASED BIT-BANG TESTER

- Cluster Test concept extended to support parametric arguments
- Leverage Test Tool DSLs to write bit-bang drivers via Boundary-Scan Register (BSR) of an FPGA, buffer or ASIC

✓ Put pressure on tool makers to give YOU access to features YOU need

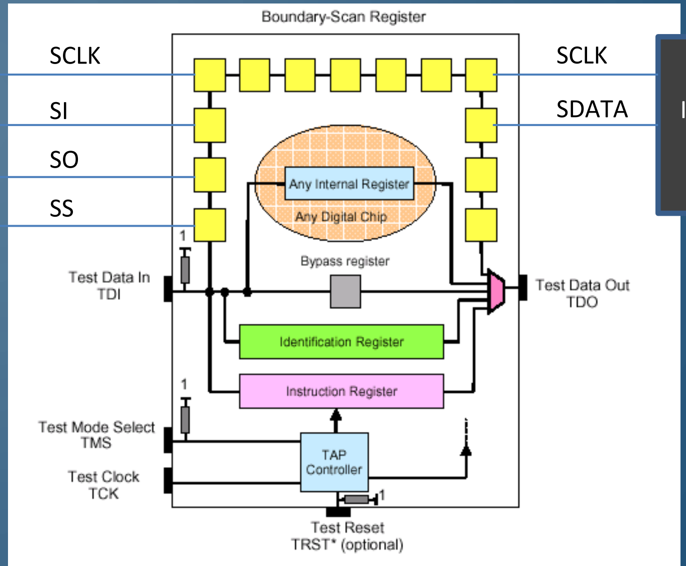
✓ YOU are the drive and innovation to what industry tooling provides

➢ **Make sure the DSL may be parameterized to allow for writing driver-like functions to reuse for similar circuits of the same kind**

FPGA

SPI Controlled Device

I2C Controlled Device



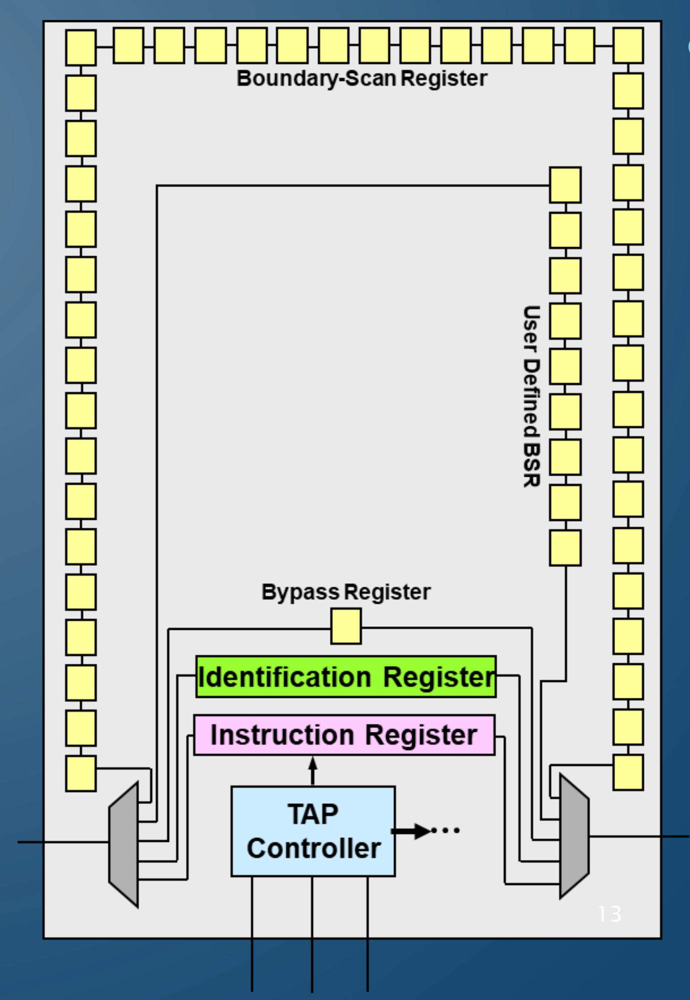
Emulate Bus Master Logic with Boundary-Scan bit-bang based program via yellow BSR cells

USER DEFINED BSR FOR LARGE FPGA

(LEARN HOW TO DESIGN FPGA LOGIC)

- Available for some FPGA designs
- Reduce number of cells in scan chain
- Use USER defined instructions
- May be included with mission logic

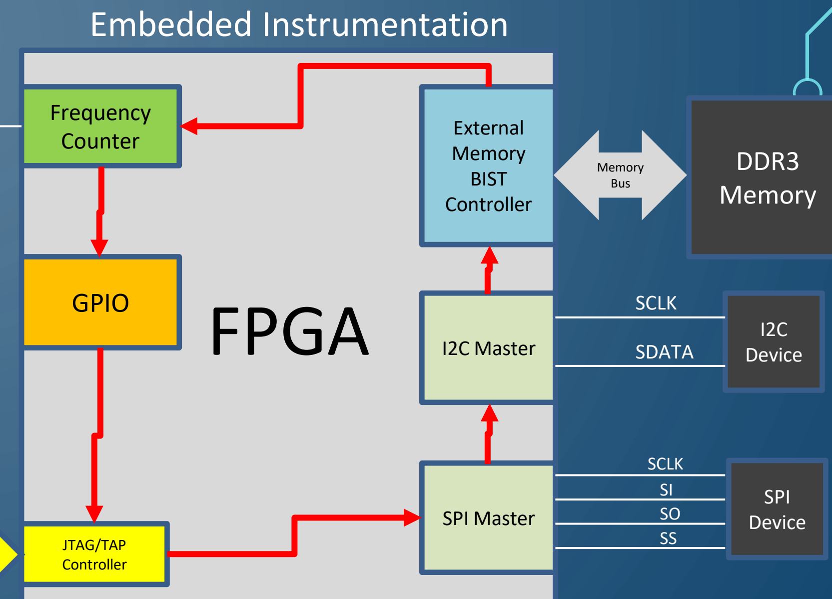
➢ The reduced cell count may significantly improve test performance



EMBEDDED INSTRUMENTATION

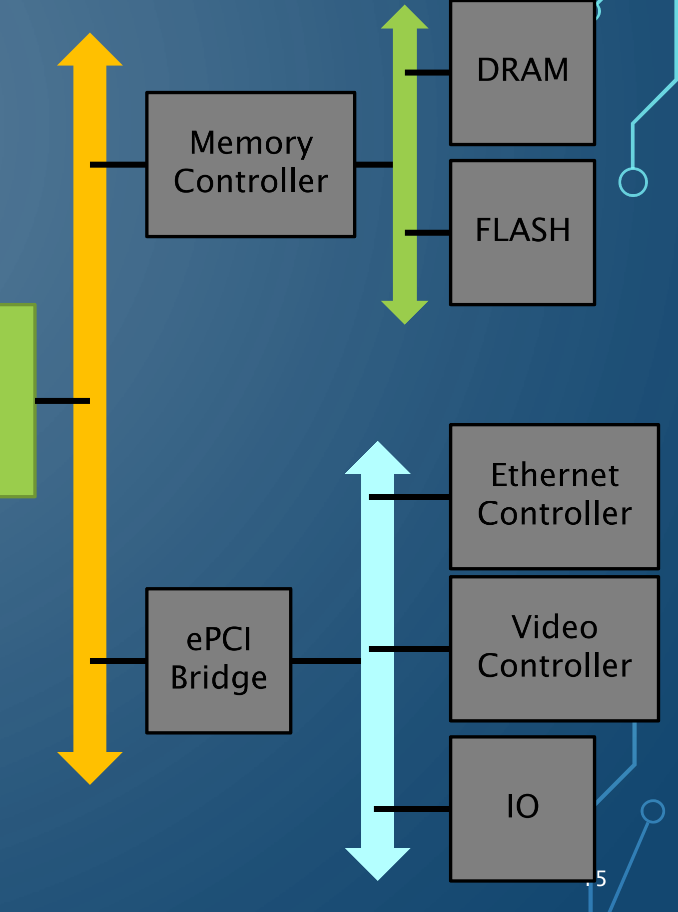
- Program functional instrumentation into an on-board FPGA to perform specialized test functions
- For manufacturing, repurpose application FPGA for test before programming application firmware
- May be useful to test interfaces at-speed

➢ **Need to weigh trade-off between programming time and test time**



PROCESSOR CONTROLLED TEST (PCT)

- Reads and writes to on-board memory and functional registers via Processor Emulation Interface (DAP)
- Exercises interfaces at-speed
- Operating System Agnostic: ATPG or runs tests scripts independent of any software on board
- Reusable test libraries across Product Units (Shared tests per device type)

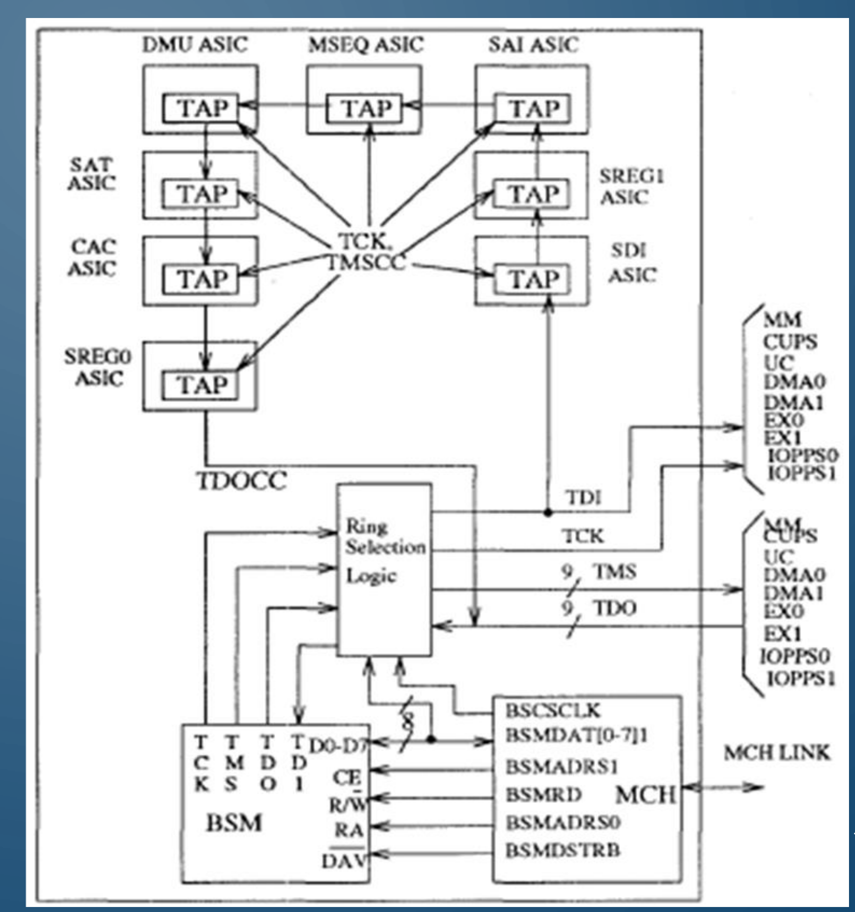


3B21D EMBEDDED TEST

- Problem Statement: Need more deterministic test and diagnosis to aid in reducing NTF/NFF
- Solution: New IEEE 1149.1 used for factory test. Could this be used "in-system" to provide factory test in the field?
- First implementation of an Embedded Boundary Scan (EBS) design (implemented in 1990)

3B21D EMBEDDED TEST

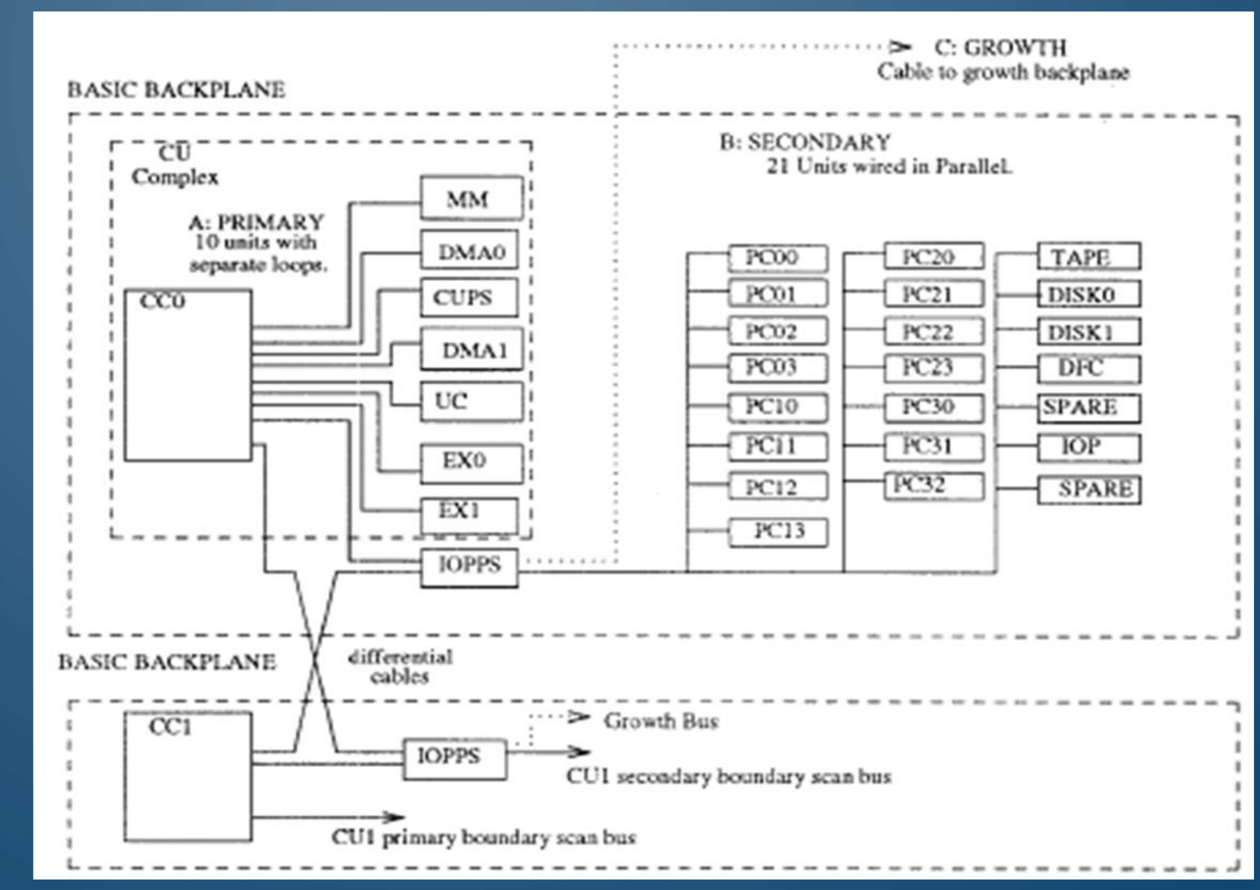
CC Circuit Board Architecture



Edward C. Behnke, **3B21D BIST/Boundary-Scan System Diagnostic Test Story,** International Test Conference Proceedings 1994, Paper 5.1

3B21D EMBEDDED TEST

3B21D Boundary-Scan Architecture (Partial Radial TAP)



Edward C. Behnke, **3B21D BIST/Boundary-Scan System Diagnostic Test Story,** International Test Conference Proceedings 1994, Paper 5.1

3B21D EMBEDDED TEST

- Implemented in 1990 (The year IEEE std 1149.1 was released)
- Reused architecture of AT&T Boundary Scan Test System (BSTS)
  - Leverage BSTS backend architecture – vector to BSM backend generator
  - BSM based controller on UNIX™ System V
- Vectors applied indirectly using BSM Domain Specific Language (DSL) scripting language
- Tests decoupled from runtime software via BSM DSL Interpreter (adding level of security)

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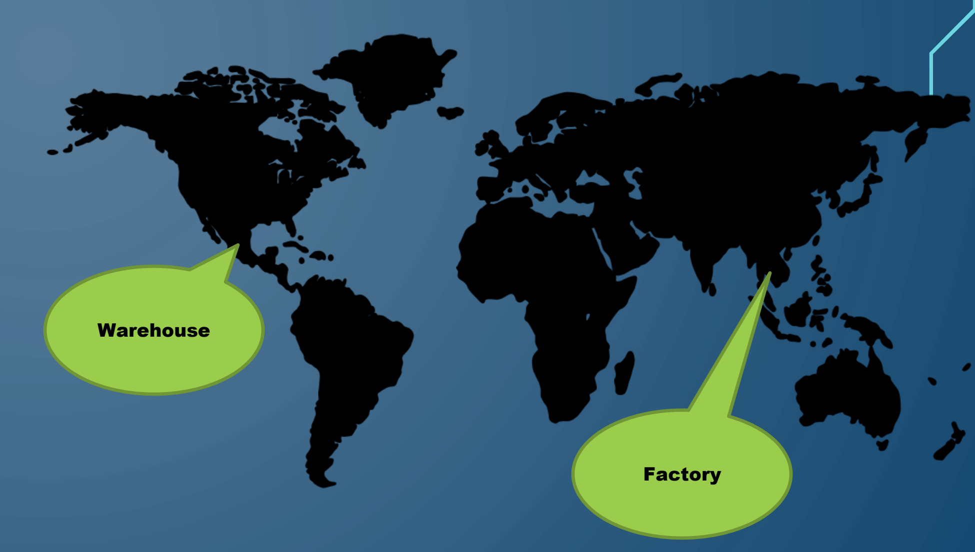
ISPCLOCK REPROGRAM FOR NEW REVISION

- Problem Statement: Board version upgrade requires clock change, but no direct field update path from application software for clock
- Solution: Fortunately, hardware designer added Multi-drop bus interface to board. System controller contains EBS utilities.

➢ Update in warehouse?



ISPCLOCK REPROGRAM FOR NEW REVISION

- New product software/firmware release
- Software update via remote update utilities
- Release requires new clock timing configuration in ispCLOCK device
- ispCLOCK only updated with IEEE 1149.1
- 3,000 boards in warehouse inventory need to be updated
- Factory only place equipped for mass updates
- No IEEE 1149.1 tester at warehouse location

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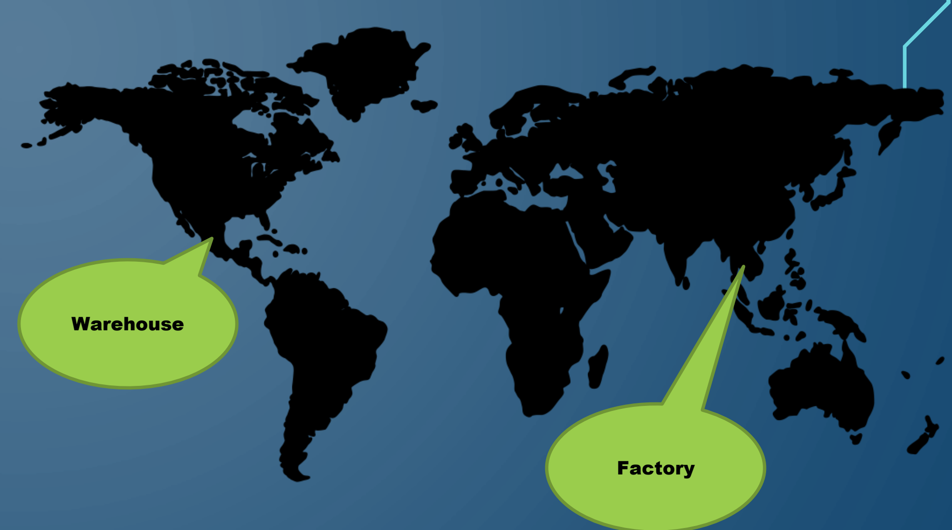
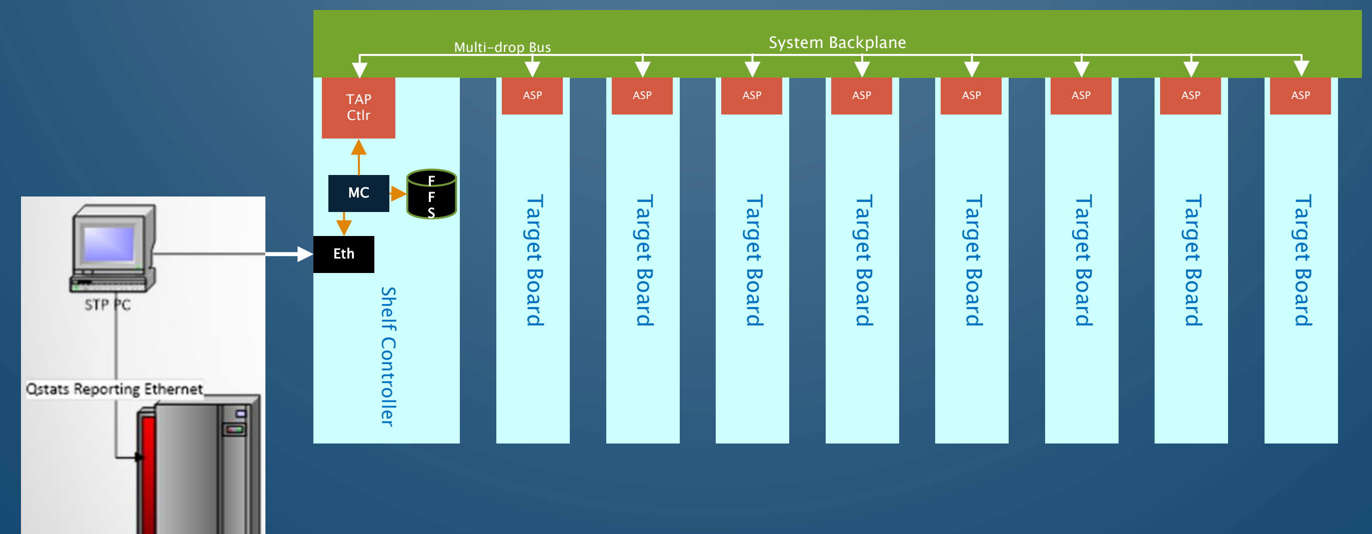


- Cost to ship inventory to factory and back + impact to current production schedule + time to reprogram + labor costs > **$1.5M est.**
- Updates must not impact current factory production to meet delivery deadlines
- Setting up BSCAN test stations at warehouse + staff required for 2 weeks > **$600,000 est.** But logistically would not fit.

ISPCLOCK REPROGRAM FOR NEW REVISION

- Warehouse also stores system frames
- Shelf Controller for system implements Embedded Boundary Scan (EBS)
- Backplane implements Multi-drop bus to target board slots needing to be updated (8 at a time)



ISPCLOCK UPDATE OUTCOME

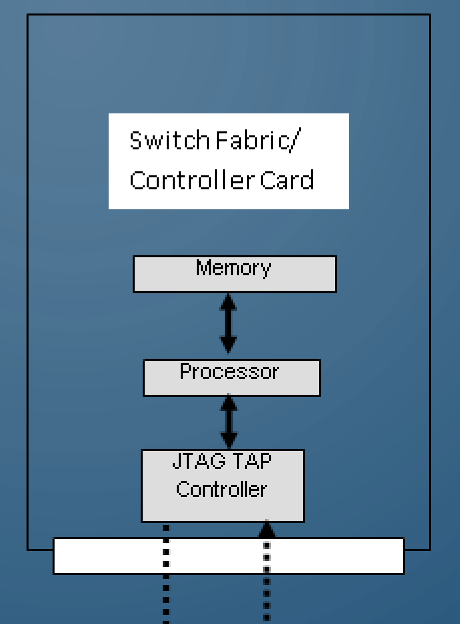
- I worked with Factory System Test Engineer to configure and modify factory software to use my EBS and track changes (3 days effort)
- Reused PC at warehouse
- Networked to Qstats server remotely
- 8 boards updated at a time
- 3 weeks to update all boards (3 shifts a day – one person per shift)
- No impact to factory production
- ~$20 hardware cost for new cables

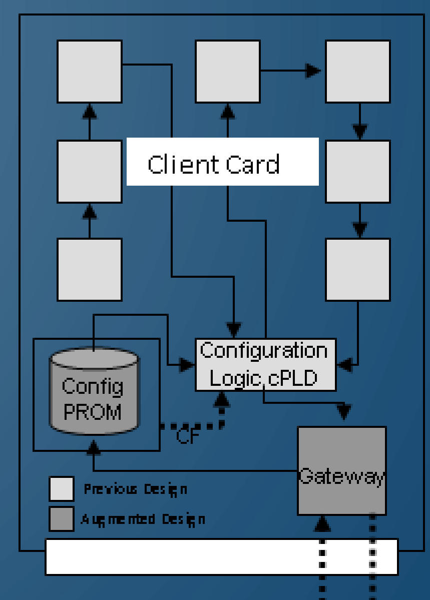
B. G. Van Treuren, B. E. Peterson and J. M. Miranda, "JTAG-based vector and chain management for system test," *IEEE International Conference on Test, 2005.*, 2005, pp. 10 pp.-787, doi: 10.1109/TEST.2005.1584041.

BOUNDARY SCAN PLUG 'N PLAY

- Vectors stored on UUT
- Tests downloaded from UUT via Multi-drop Test Bus
- Decouple tests from system software using DSL (TFCL in my case)

➢ New UUTs automatically supported by Controller Card without changes to the system software





Backplane Multi-drop Test Bus

ASIC WORKAROUND

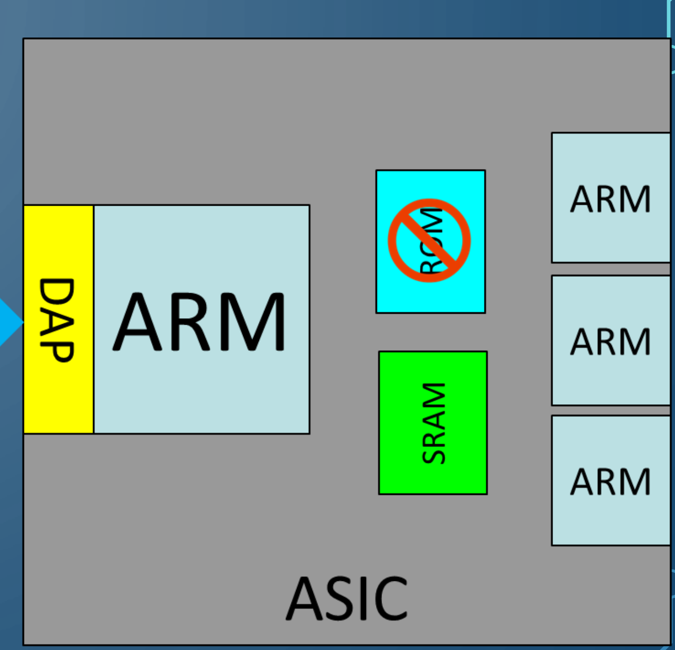
Problem Statement: Foundry building ASIC broke boot ROM for ARM core. Thus, unable to prove-in first batch.

Solution: Use ARM DAP to program ARM SRAM for alternate boot as a workaround.

Issue1: Emulator is expensive and does not provide IEEE 1149.1 sequences to program DAP with alternate tools.

Issue2: Some test boards use multiple ASICs in parallel for load balancing, so a multiplicity of ASICs need to boot for some designs.

JTAG Interface



ASIC WORKAROUND

- ASIC emulated with HASP hardware simulation and able to capture TAP signal states during DAP programming.
- Write converter from TAP signal logs to SVF.
- Use Raspberry Pi as test programming vehicle to provide a low cost tester and prove-in concept using FPGA on test board to boot all instances at power-up.
- White wire test boards to use FPGA ARM based embedded boundary-scan to play SVF for each site to boot.
- Offset each of the ASIC vector files using SVF HDR and TLR statements to reuse common SVF vectors.

➢ASIC prove-in continued with workaround in 4 days after defect discovered.

INSIGHTS LEARNED

- Think outside the test box
- Look for ways to improve your testing and coverage on every job
- Get to know your hardware designers very well
- Be an evangelist for DfT
- Learn different perspectives from other industries
- Get involved with standards development
- Expand your knowledge about test techniques others use (read more)
- NEVER STOP LEARNING!

OTHER INDUSTRIES

- Software community (Pattern Languages and DSLs)
- Automotive Test (distributed architecture)
- Avionics (small interconnected systems – hard to access)

CLOSING MESSAGE

What makes a technology successful (or not)?

It's Up to YOU!